In the Specification:

Please amend paragraphs 0053 and 0068 of the specification as indicated below.

[0053] FIG. 2d shows the device 100 after that in the following steps the dielectric layer 11 is partially etched away, and a layer of electrically conductive material is provided to define a top electrode 44 of the planar capacitor 40, the second conductive surface 24 of the vertical capacitor 20, the contact 25 to the first conductive surface 22 [[23]], and the filling of the first part 31 of the vertical interconnect 30. Part of the dielectric layer 11 forms a dielectric 43 of the planar capacitor 40. In this example, use is made of a 0.5 μm thick conductive layer of n-type in situ doped polysilicon. It was deposited by LPCVD from SiH_4 diluted PH_3. After a furnace anneal step of 30 minutes at 1000° C. the conductivity of the polysilicon is in the order of 1 mΩ/cm. Due to the use of parallel trenches 311, 312, 313 for the first part 31 of the vertical interconnect 30, this conductivity does not lead to an impedance that is too high. The trenches 311, 312, 313 are filled. In this filling process the polysilicon is first deposited on the side-walls and then grows in the kinetic regime. Although not explicitly shown, the polysilicon layer 11 is also used as seed layer for the wiring pattern on the second side 2 of the substrate. This wiring pattern is grown by electroplating thereafter. Alternatively, use can be made of the polysilicon as seed layer also in the first part 31 of the interconnect 30. The trenches 311, 312, 313 in the first part will be completely filled, even if the seed material is present only at their ends.

[0068] This system is assembled in the following manner. Metal has been applied at the bond pad areas of both the device 100 and the active device 200. The device 100 is thereto provided with an underfill metal, such as a Ni or TiW layer on top of the bond pads. The metal is joined in a thermal compression treatment. Thereafter an underfill material is provided so as to fill the area between the device 100 and the active device 200. This underfill acts as a protective layer against moisture and other chemical contamination layer, which layer is known per se. The lead-frame 310 ~~210~~ comprises a first and a second electrically conductive layer of Cu. The lead frame 310 ~~210~~ is formed by skillfully etching it with a semi-etching technique, first from the first side and then

from the second side or the other way around. This results in a heat sink 312 and in leads 311, while the heat sink 312 is also a contact surface. The heat sink 312 is customarily connected to the rest of the lead frame 310 by means of four wires. There is an open space under the leads 311, which is filled with a molding material. This provides a mechanical anchoring of the leadframe in the molding material. On the heatsink 312 a conductive adhesive is applied i.e. a silver containing glass epoxy adhesive. Solder dots are provided on the leads 311, for example, by printing with a stencil. The solder is here a low-melting SAC solder which contains over 96% Sn, 3% Ag and about 0.5% Cu.